THE INVENTION CLAIMED IS:

1. A method of forming an integrated circuit comprising:

providing a semiconductor substrate;

forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming at least one raised source/drain layer on the semiconductor substrate adjacent the gate and the gate dielectric;

forming at least one amorphized shallow source/drain extension implanted region in the raised source/drain layer and the semiconductor substrate therebeneath; and

recrystalizing the amorphized region to form at least one shallow source/drain extension having residual recrystallization damage elevated into the raised source/drain layer.

2. The method as claimed in claim 1 wherein the raised source/drain layer is formed by solid epitaxy growth.

3. The method as claimed in claim 1 wherein forming at least one amorphized shallow source/drain extension implanted region further comprises amorphizing the region by a damaging ion implantation of an inert species.

4. The method as claimed in claim 1 further comprising:

forming a curved sidewall spacer adjacent the gate dielectric and the gate, with portions of the raised source/drain layer having a lateral extent greater than that of the curved sidewall spacer; and

removing portions of the raised source/drain layer extending laterally beyond the curved sidewall spacer.

5. The method as claimed in claim 1 further comprising:

forming a deep source/drain junction augmenting the shallow source/drain extension;

forming a silicide on the deep source/drain junction and on the gate;

depositing an interlayer dielectric above the semiconductor substrate; and

forming contacts in the interlayer dielectric to the silicide.

6. A method of forming an integrated circuit comprising:

providing a semiconductor substrate;

forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming raised source/drain layers on the surface of the semiconductor substrate on each side of and adjacent the gate and the gate dielectric;

implanting the raised source/drain layers and the semiconductor substrate therebeneath;

amorphizing the implanted raised source/drain layers and the implanted semiconductor substrate therebeneath to form amorphized shallow source/drain extension implanted regions; and

recrystalizing the amorphized shallow source/drain extension implanted regions with solid phase epitaxy to form shallow source/drain extensions having residual recrystallization damage from the solid phase epitaxy elevated into the raised source/drain layers above the surface of the semiconductor substrate.

7. The method as claimed in claim 6 wherein the raised source/drain layers are formed by solid epitaxy growth.

8. The method as claimed in claim 6 wherein amorphizing the implanted raised source/drain layers and the implanted semiconductor substrate therebeneath further comprises amorphizing by a damaging ion implantation of an inert species.

9. The method as claimed in claim 6 further comprising:

forming a curved sidewall spacer adjacent the gate dielectric and the gate, with portions of the raised source/drain layers having a lateral extent greater than that of the curved sidewall spacer; and

removing portions of the raised source/drain layers extending laterally beyond the curved sidewall spacer.

10. The method as claimed in claim 6 further comprising:

forming deep source/drain junctions augmenting the shallow source/drain extensions;

forming a silicide on the deep source/drain junctions and on the gate;

depositing an interlayer dielectric above the semiconductor substrate; and

forming contacts in the interlayer dielectric to the silicide.

11. An integrated circuit comprising:

a semiconductor substrate;

a gate dielectric on the semiconductor substrate;

a gate on the gate dielectric;

at least one raised source/drain layer on the semiconductor substrate adjacent the gate and the gate dielectric; and

at least one shallow source/drain extension having residual recrystallization damage elevated into the raised source/drain layer.

12. The integrated circuit as claimed in claim 11 wherein the raised source/drain layer is a solid epitaxy growth layer.

13. The integrated circuit as claimed in claim 11 wherein the shallow source/drain extension is formed in a shallow source/drain extension implanted region amorphized by an inert species damaging ion implantation.

14. The integrated circuit as claimed in claim 11 further comprising a curved sidewall spacer over the raised source/drain layer adjacent the gate dielectric and the gate.

15. The integrated circuit as claimed in claim 11 further comprising:

a deep source/drain junction augmenting the shallow source/drain extension;

a silicide on the deep source/drain junction and on the gate;

an interlayer dielectric above the semiconductor substrate; and

contacts in the interlayer dielectric to the silicide.

16. An integrated circuit comprising:

a semiconductor substrate;

a gate dielectric on the semiconductor substrate;

a gate on the gate dielectric;

raised source/drain layers on the surface of the semiconductor substrate on each side of and adjacent the gate and the gate dielectric; and

implanted recrystallized shallow source/drain extensions having residual recrystallization damage elevated into the raised source/drain layers above the surface of the semiconductor substrate.

17. The integrated circuit as claimed in claim 16 wherein the raised source/drain layers are solid epitaxy growth layers.

18. The integrated circuit as claimed in claim 16 wherein the shallow source/drain extensions are formed in shallow source/drain extension implanted regions amorphized by an inert species damaging ion implantation.

19. The integrated circuit as claimed in claim 16 further comprising a curved sidewall spacer over the raised source/drain layers adjacent the gate dielectric and the gate.

20. The integrated circuit as claimed in claim 16 further comprising:
deep source/drain junctions augmenting the shallow source/drain extensions;
a silicide on the deep source/drain junctions and on the gate;
an interlayer dielectric above the semiconductor substrate; and
contacts in the interlayer dielectric to the silicide.